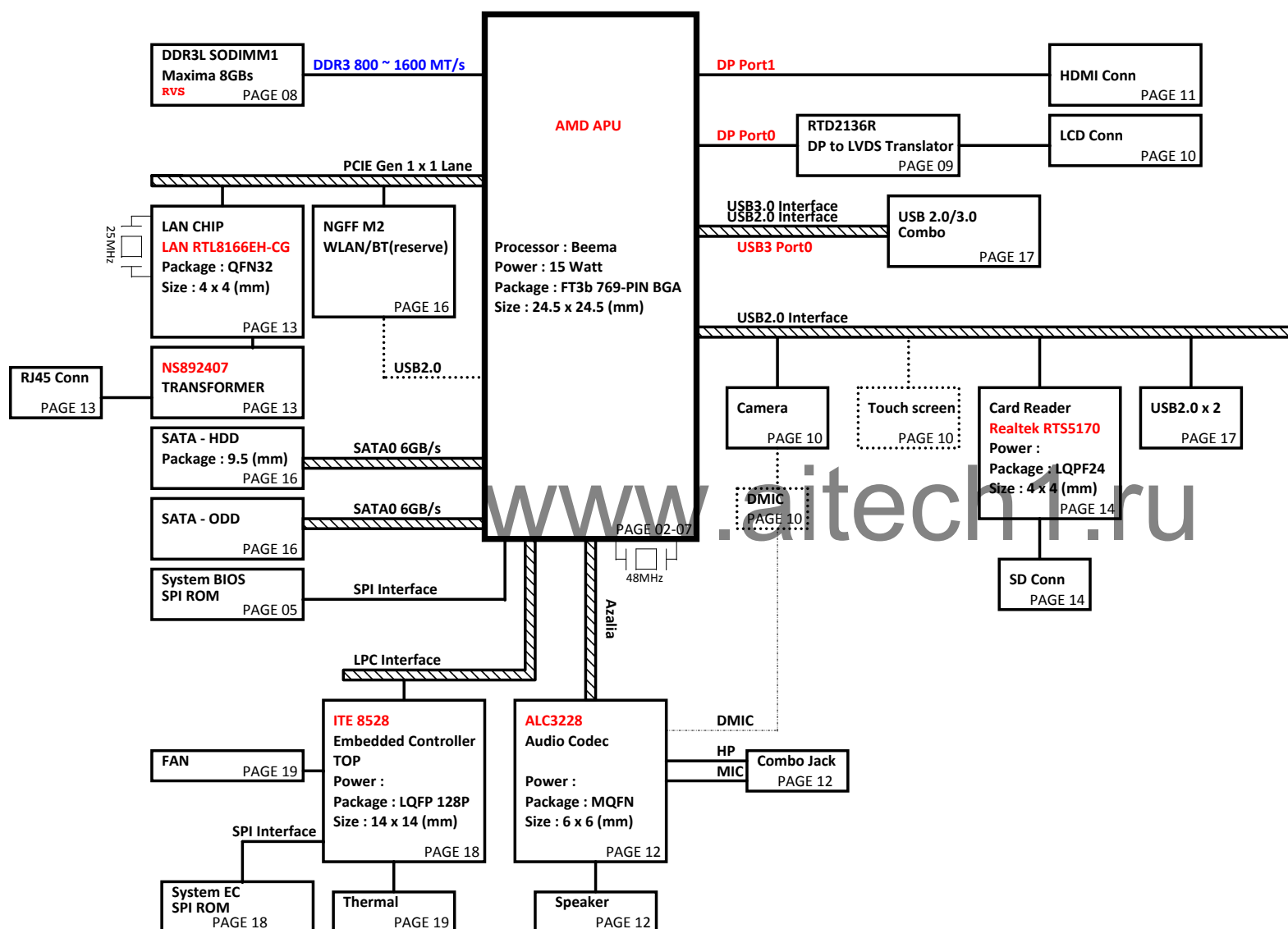


Icebreaker AMD Beema UMA (19.5")



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1 (HIGH)
LAYER 4 : IN2 (LOW)
LAYER 5 : SVCC
LAYER 6 : GND

Power Source

DC IN Circuit

PAGE 21

RT7238B / RT7238C

System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

PAGE 22

RT8231BGQW

System Memory Power (+1.35VSUS/
+0.65V_DDR_VTT)

PAGE 23

APW8824 / APW8824

Processor Power
(+0.95VS5/+1.5VS5)

PAGE 24

AOZ1267QI-02 / RT8068AZQW

Processor Power
(+0.95V/+1.8VS5)

PAGE 25

ISL62771

Processor Power
(+VCC_CORE/+VDDNB_CORE)

PAGE 26,27

APL3523A * 3

Load switch
(+3V/+5V/+1.5V/+1.8V)

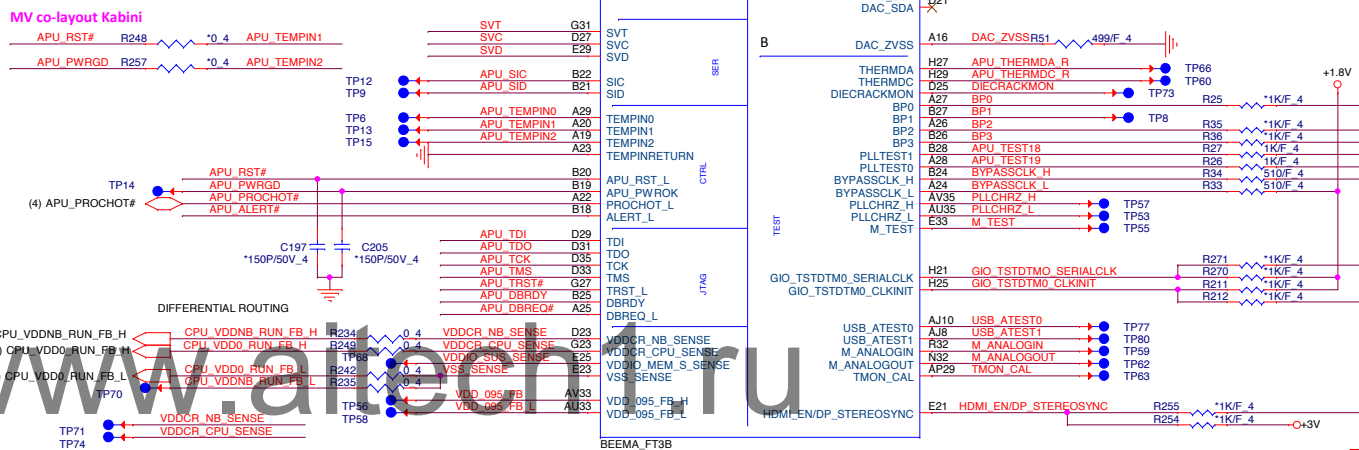
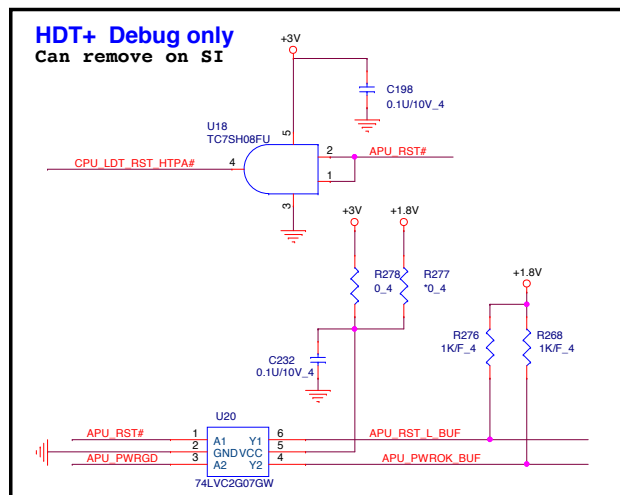
PAGE 28

OZ554

Panel Backlight Circuit

PAGE 29





close to HDT debug HEADER

+1.8V

APU TDI R180 1K/4

APU TCK R178 1K/4

APU TMS R179 1K/4

APU TRST# R181 1K/4

APU DBREQ# R177 1K/4

Pinout diagram for the DB stage of the 88511-2001-2004 connector. The diagram shows a 20-pin connector with pins numbered 1 to 20. Pin 1 is ground. Pin 2 is APU PWROK_BUF. Pin 3 is APU TDO. Pin 4 is APU TRST#. Pin 5 is APU TDI. Pin 6 is APU TMS. Pin 7 is APU TCK. Pin 8 is APU DBRDY. Pin 9 is APU DBREQ#. Pin 10 is CPU LDT_RST_HTPA#. Pin 11 is APU RST_L_BUF. Pin 12 is APU TEST19. Pin 13 is APU TEST18. Pin 14 is +1.8V. Pin 15 is TP51. Pin 16 is ground. Pin 17 is APU DBREQ#. Pin 18 is APU TDO. Pin 19 is APU TRST#. Pin 20 is APU TDI. The diagram also shows a ground symbol connected to pin 1 and a +1.8V source connected to pin 14.

Thermal Sensor

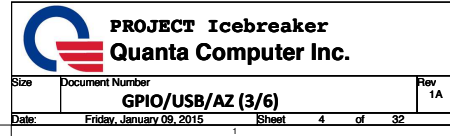
(18,19) THERM_CLK \Rightarrow THERM_CLK R38 0.4 APU_SIC

(18,19) THERM_DAT \Rightarrow THERM_DAT R37 0.4 APU_SID

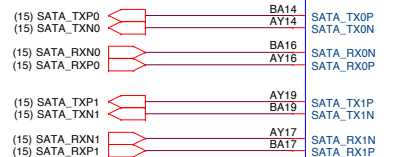
+3V

R31 1K/F_4 R32 1K/F_4

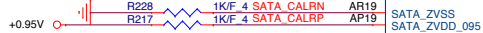
VFX MODE		VID Override table (VDD)
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



SATA HDD



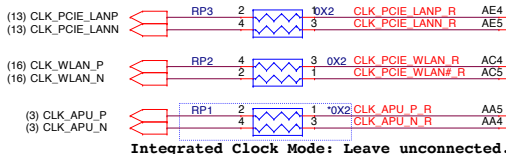
SATA ODD



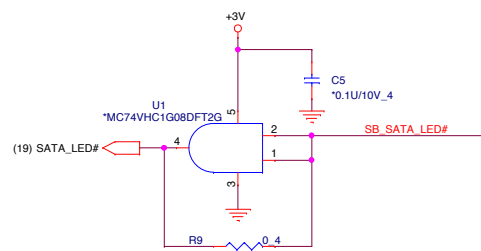
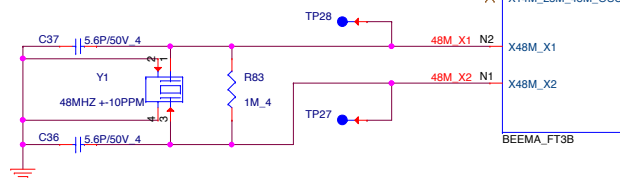
Use with external clock generator only

Integrated Clock Mode:
Leave unconnected.

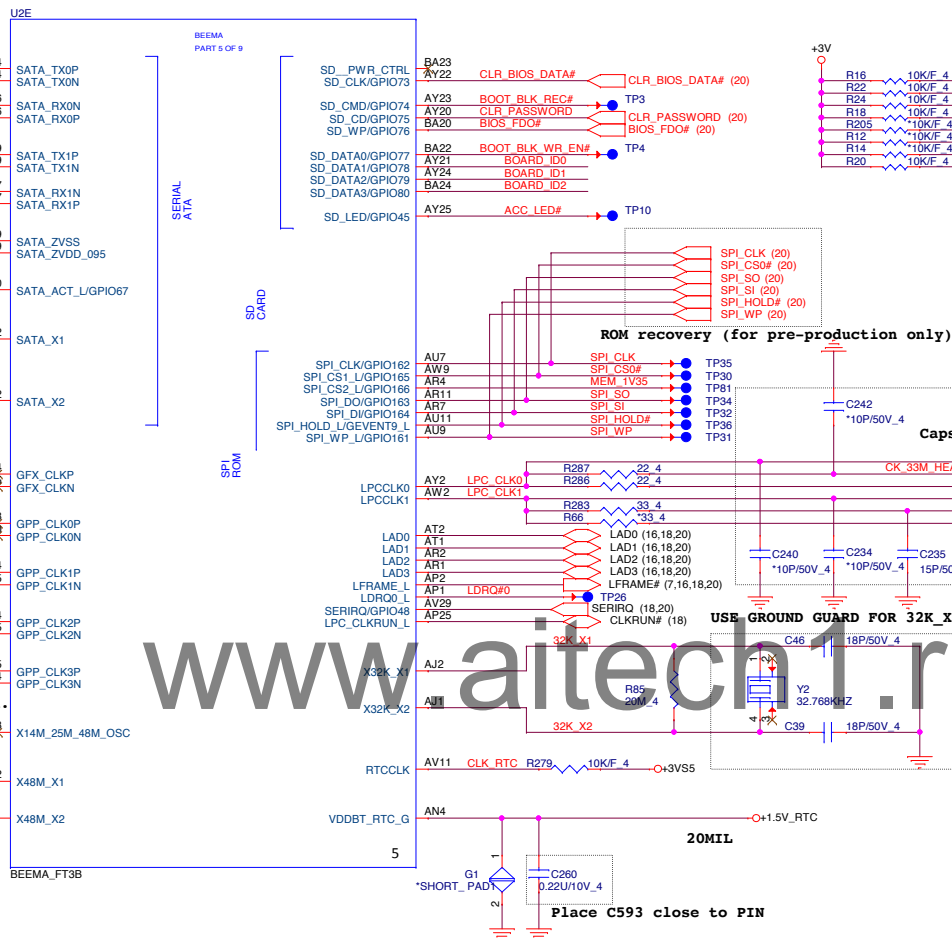
Remove for UMA



Integrated Clock Mode: Leave unconnected.



CMOS clear need to check



ROM recovery (for pre-production only)

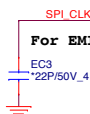
Caps closed to APU

USE GROUND GUARD FOR 32K_X1 AND 32K_X2

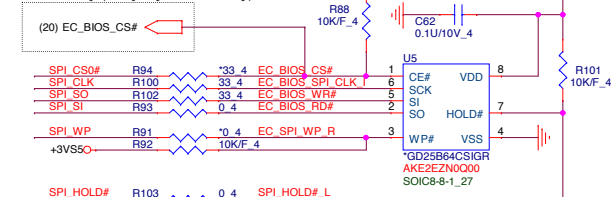
Place C593 close to PIN

APU SPI ROM 8M SPI EC ROM

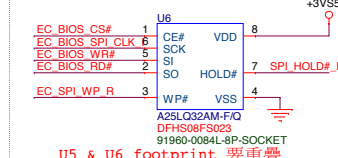
Vender	Size	P/N
GGD	8M	AKE2EZNOQ00
WND	8M	AKE3EFPON07
EON	8M	AKE3EZNOQ01
Socket		DFHS08FS023



ROM recovery (for pre-production only)



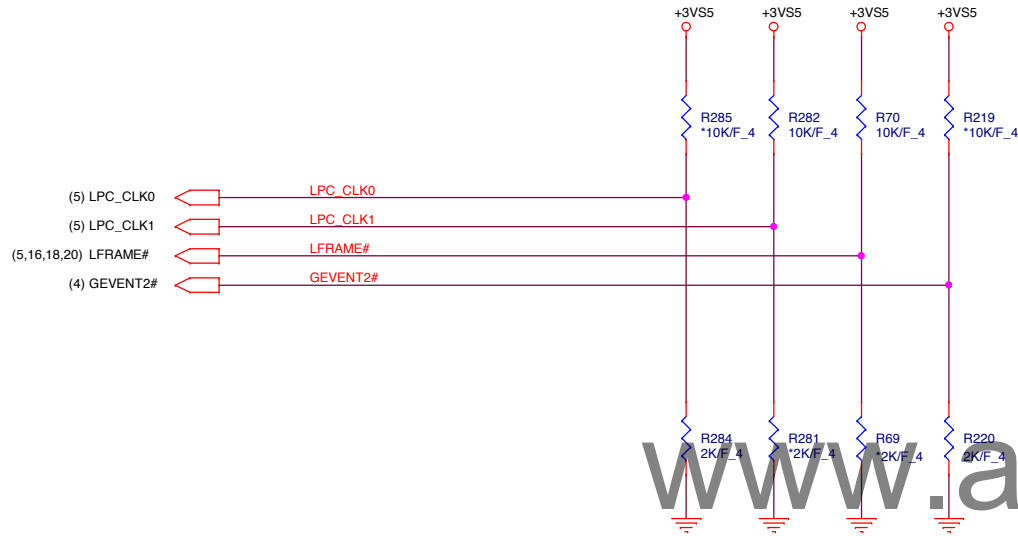
SPI ROM Socket



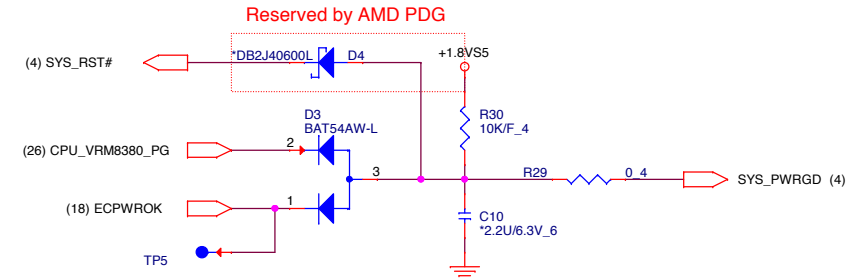


STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

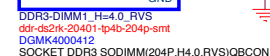


SYS_PWRGD



REQUIRED STRAPS

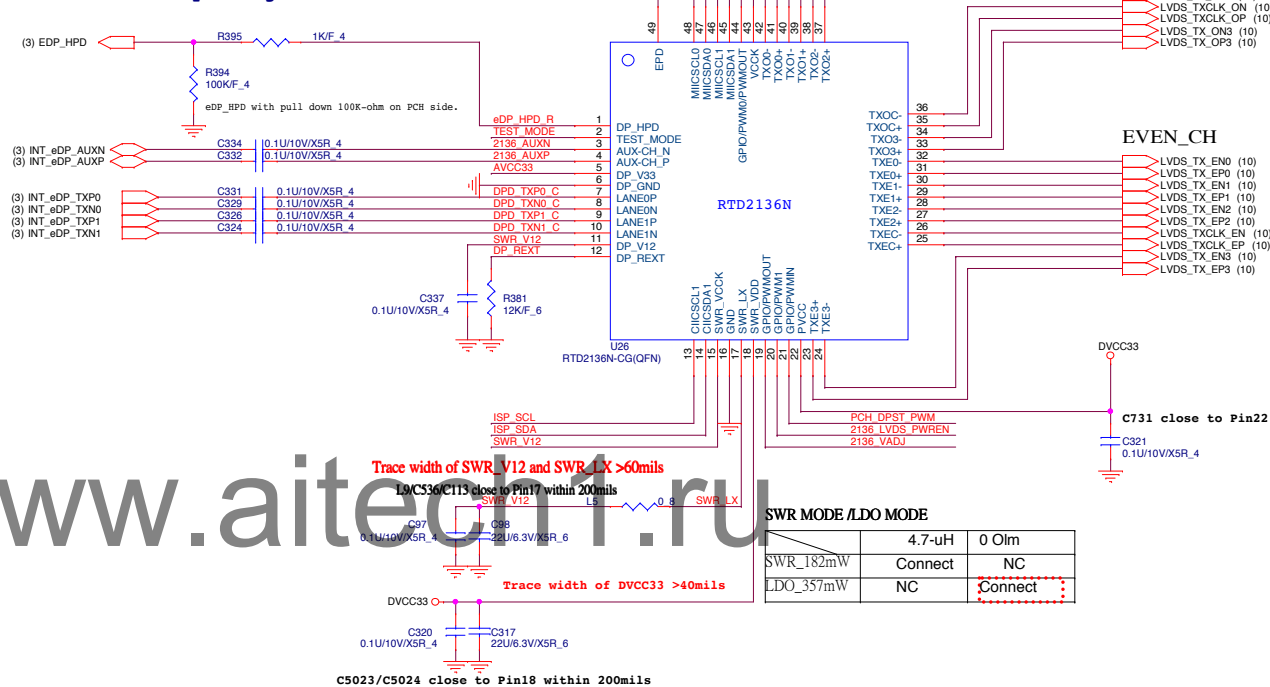
	LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT



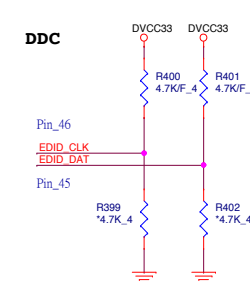
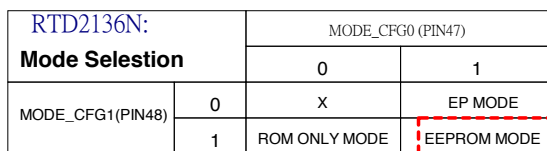
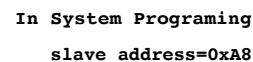
Size	Document Number	Rev
	DDR3 DIMM0-RVS (4.0H)	1A
Date:	Friday, January 09, 2015	Sheet 8 of 32

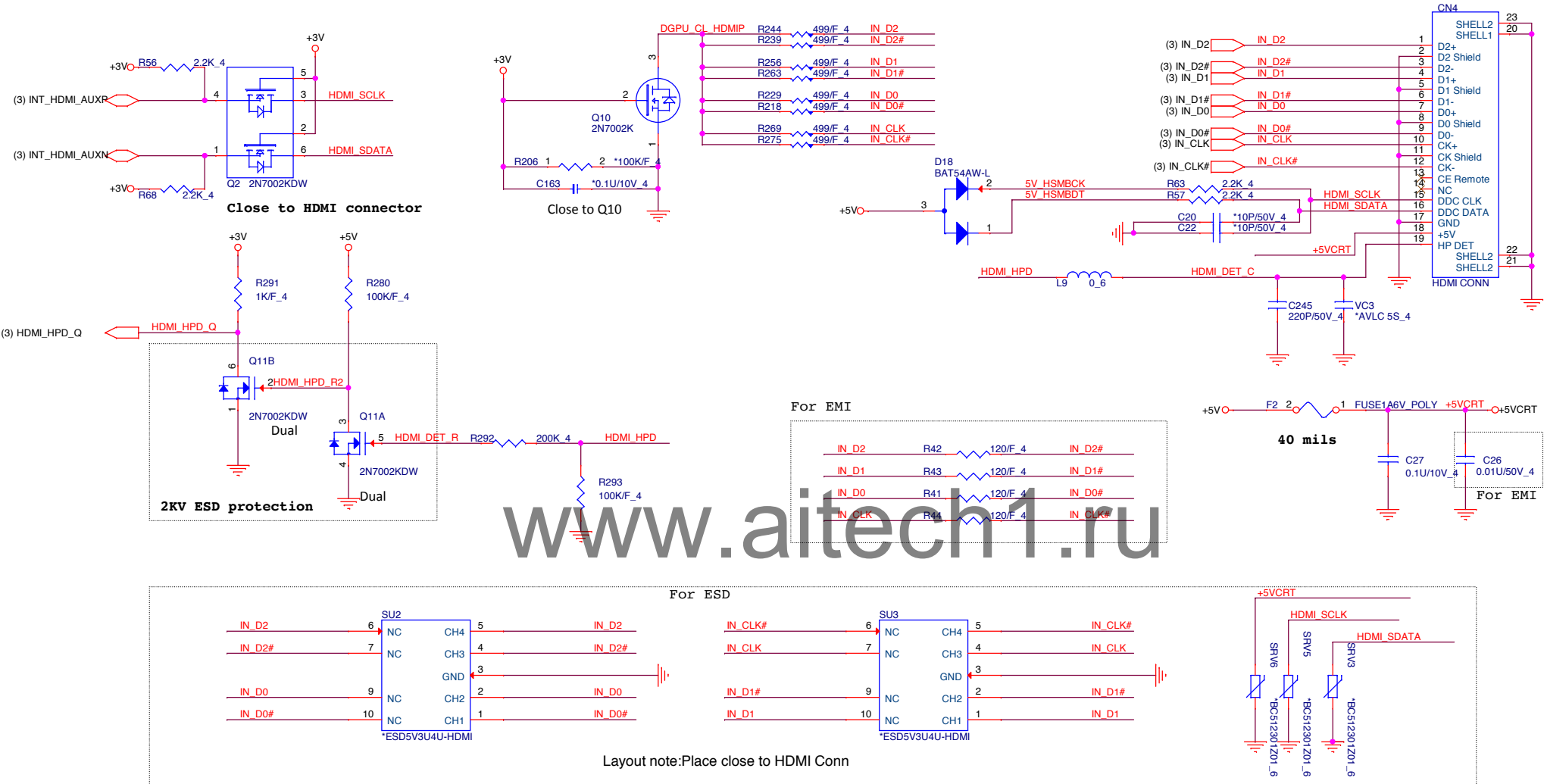
09

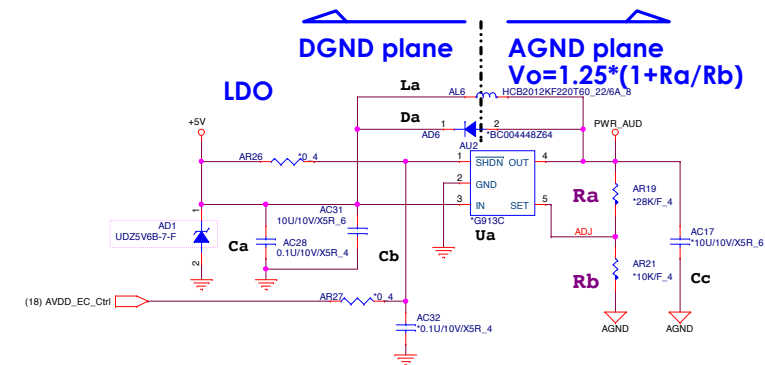
DP input signals



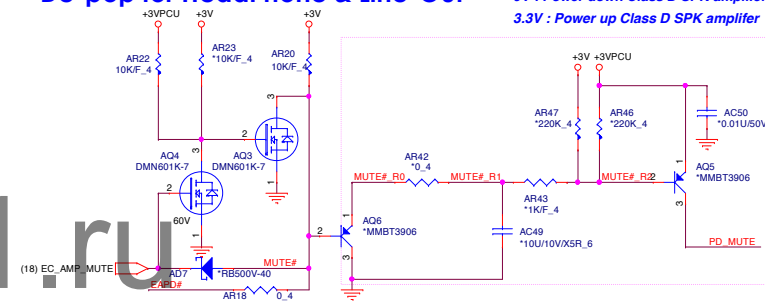
SWR MODE /LDO MODE		
	4.7-uH	0 Ohm
SWR_182mW	Connect	NC
LDO_357mW	NC	Connect



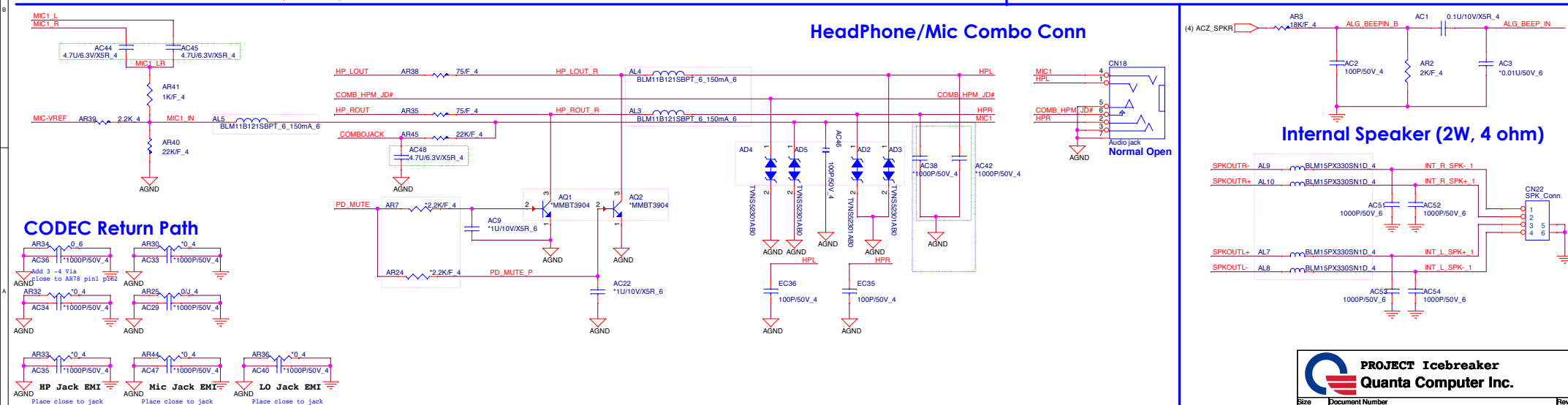




0V : Power down Class D SPK amplifier
3.3V : Power up Class D SPK amplifier

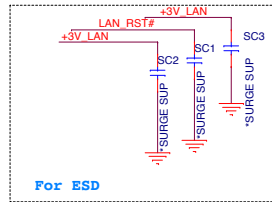
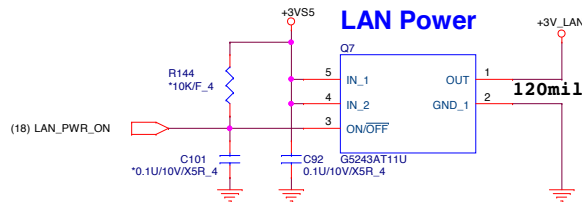


Internal Speaker (2W, 4 ohm)



For EMI 0 - 22 ohm

(3,4,5,6,8,9,10,11,12,14,15,18,19,20,26,28) +3V
(4,5,6,7,10,16,18,19,20,21,22,24,25,28) +3VSS



13

if ISOLATEB pin pull-low, the LAN chip will not drive its PCI-E outputs (excluding PCIE_WAKE# pin)

Power trace Layout 宽度 > 60mil

For 10/100

Place Cc, Cd

close to each VDD10 pin-- 8, 30

>60mil

>60mil

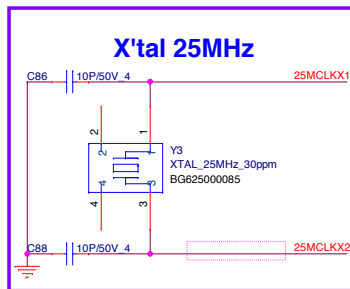
Trace < 30 mil
Width > 60 mil

For 10/100

NA: Ca, Cb
Stuff La (ohm), Cz

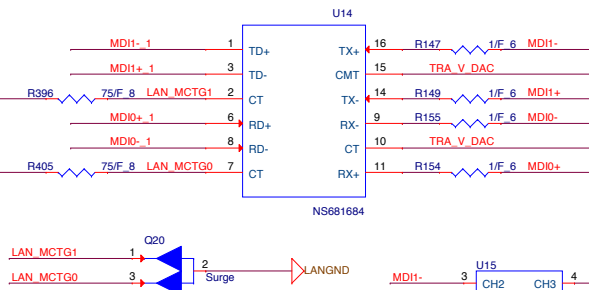
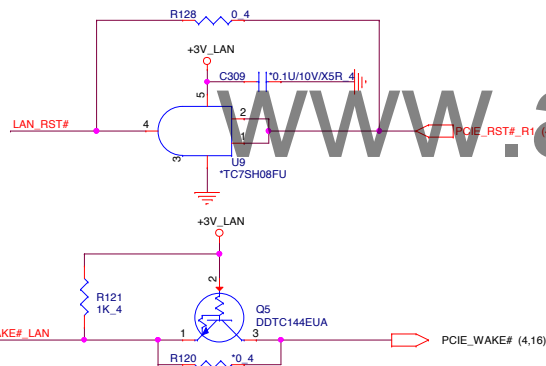
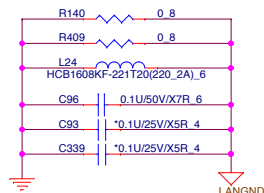
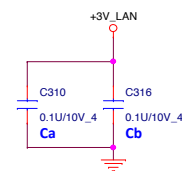
For 10/100

Place Cg, Ch close to each VDD10 pin-- 30 (reserve)



For 10/100

Stuff Ca and Cb only, close to each VDD33 pin-- 23, 32



Please add 9 GND Vias connection with thermal PAD

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

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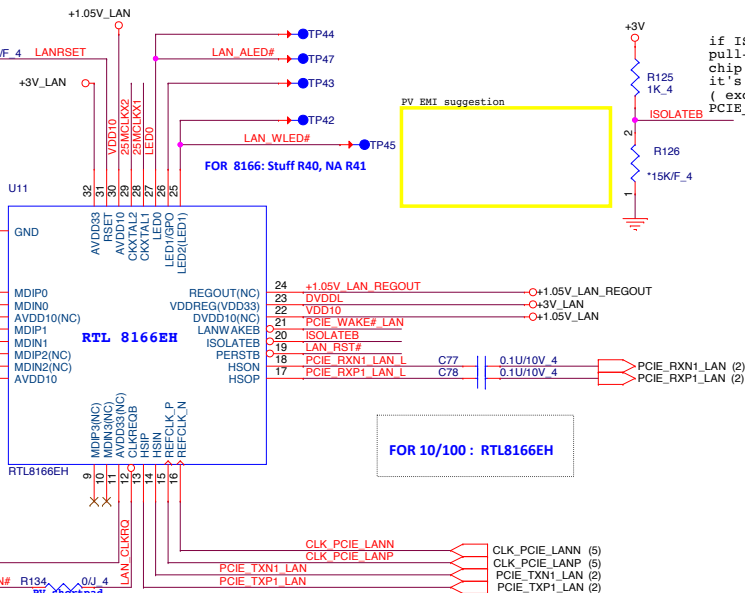
MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

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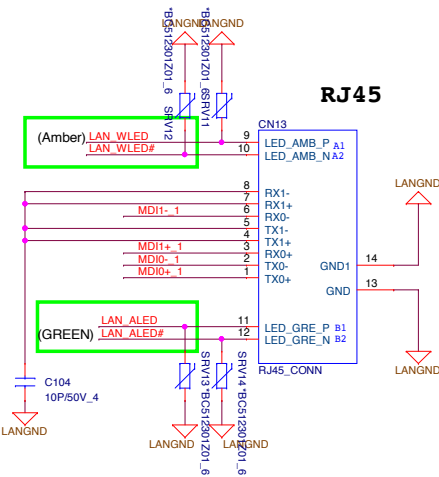
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MDIO+ 1 MDIO- 2 VDD10 (NC) 3 MDIO+ 4 MDIO- 5 MDIO+ 6 MDIO- 7 MDIO+ 8

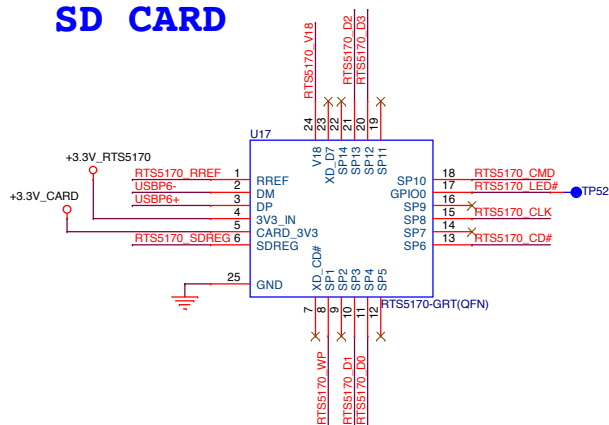


FOR 10/100 : RTL8166EH

LAN conn



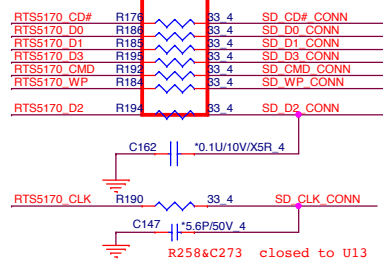
SD CARD



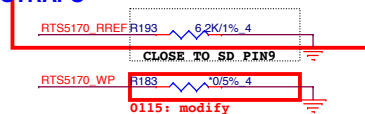
CARD PCIE INTERFACE

EXT.SD (4) USBP6+
(4) USBP6-

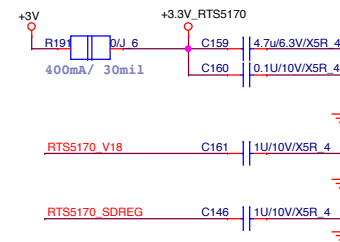
CO-LAY with SoC



HW STRAPS

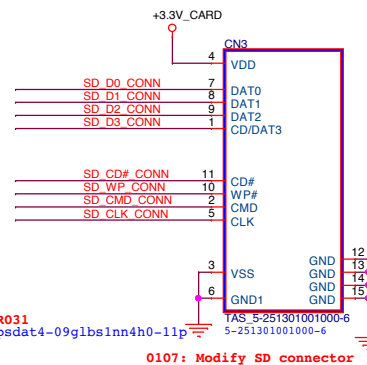
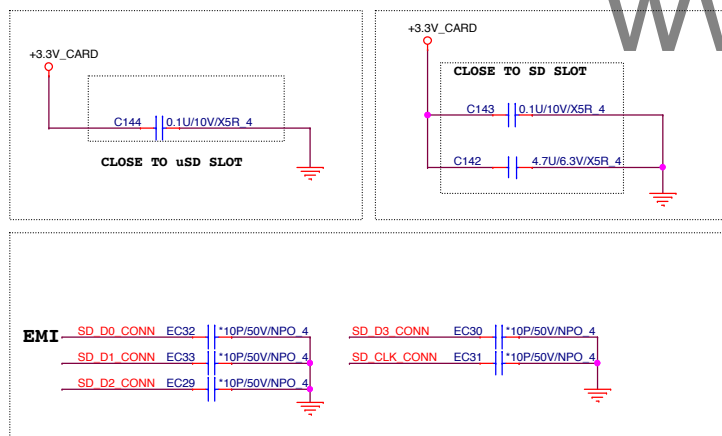


CARD POWER



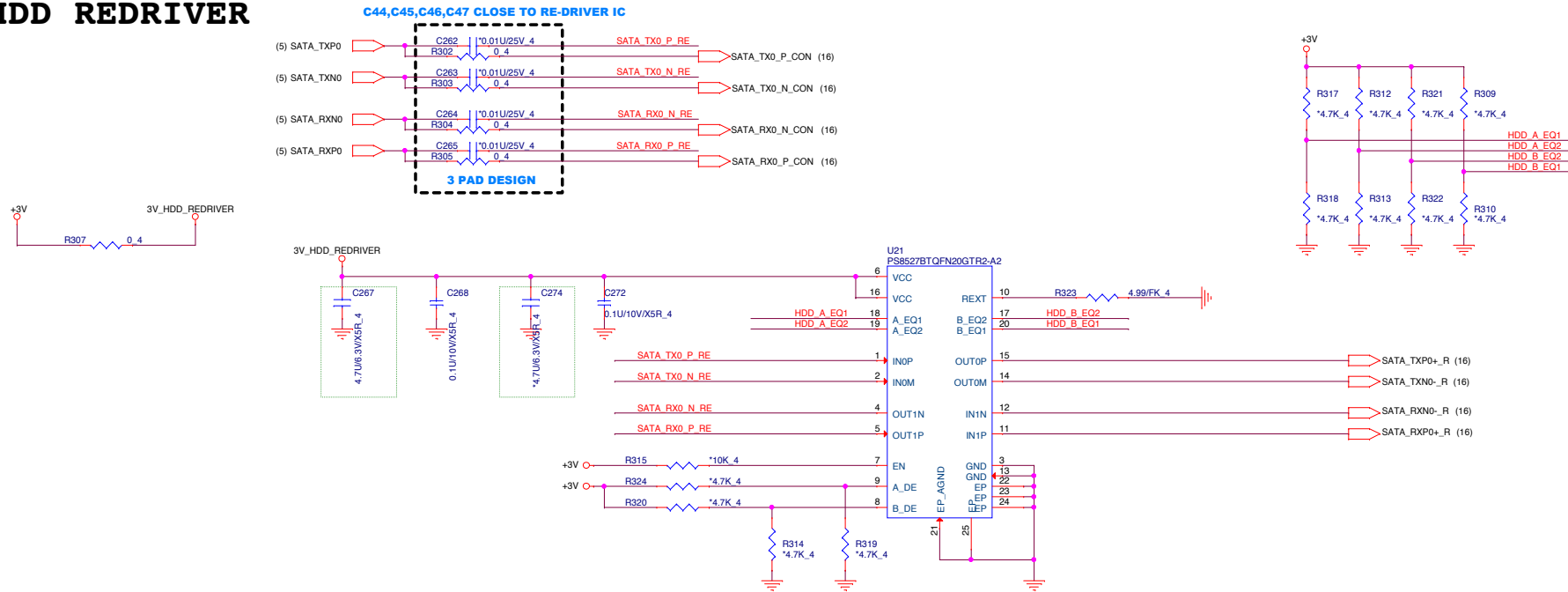
www.aitech1.ru
This is full size SD card

SD SLOT

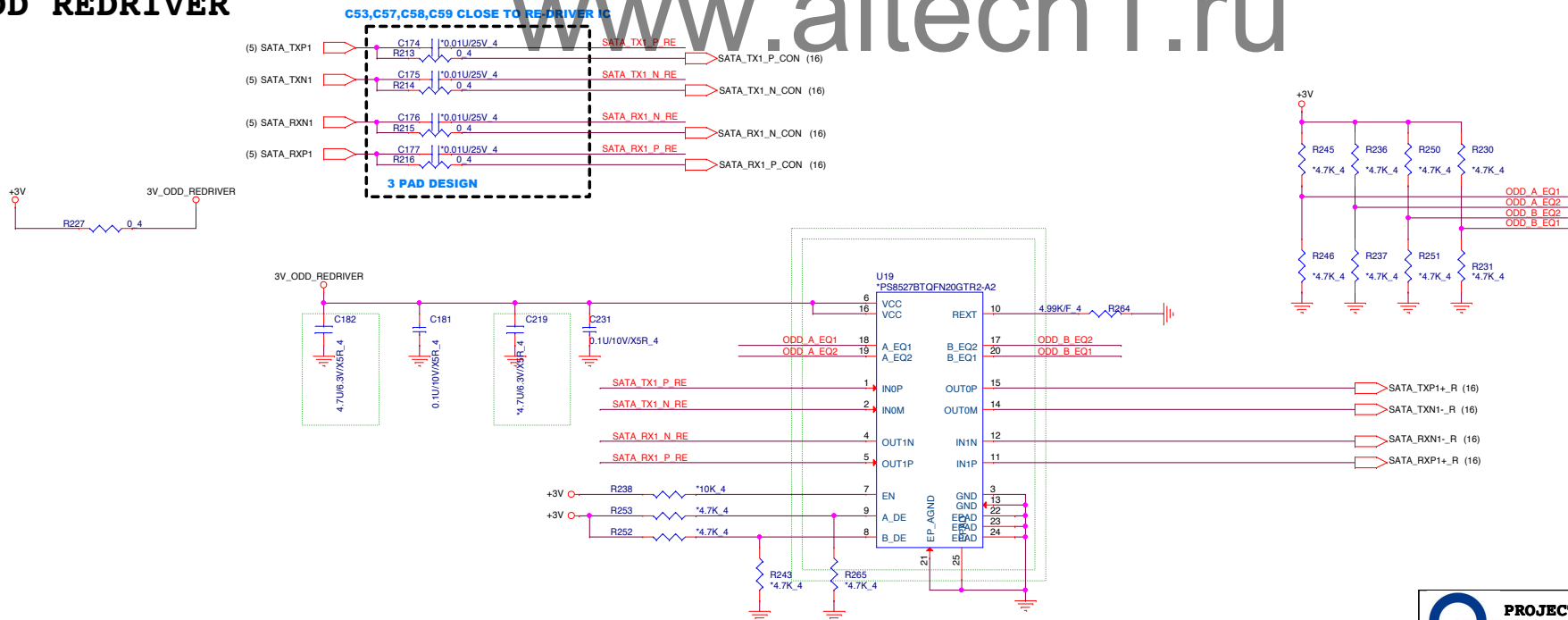


DFHD11MR031
sdcard-psdat4-09glbsl1nn4h0-11p
0107: Modify SD connector

HDD REDRIVER



ODD REDRIVER



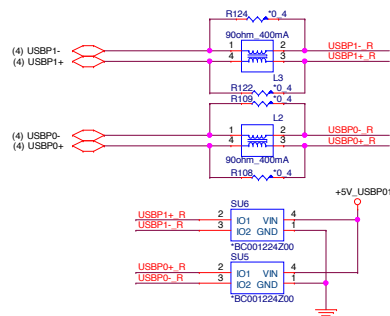


ODD

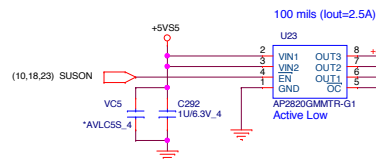
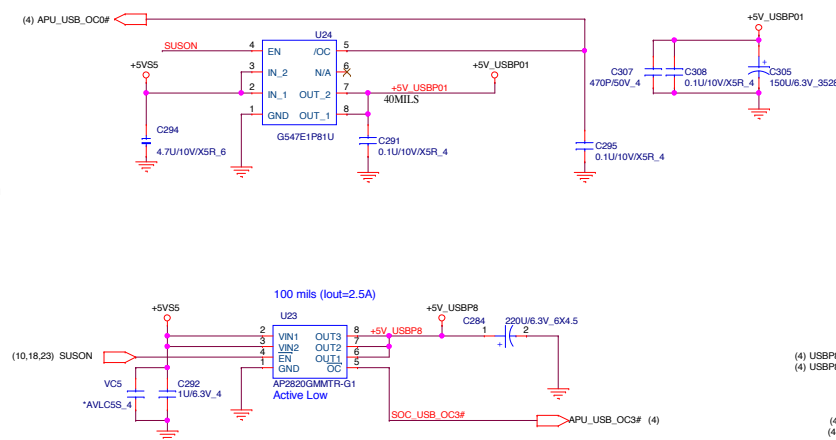


PLACE SATA AC COUPLING CAPS CLOSE TO Connector

(10,19,21,22,23,25,26,28) +5VSS



USD protection diodes for ESD,
as close as possible to USB connector pins.



(10,18,23) SUSON

*AVLCSS_4

AP2820GMM/T-R-G1

Active Low

SOC_USB_OC3#

APU_USB_OC3# (4)

100 mils (Iout=2.5A)

C294

220uF/6.3V_6X4.5

+5V_USBPO1

C292

1uF/6.3V_4

5VSS

SUSON

VIN1

VIN2

EN

OUT3

OUT2

OUT1

OC

GND

+5V_USBPO1

C294

220uF/6.3V_6X4.5

5VSS

SUSON

VIN1

VIN2

EN

OUT3

OUT2

OUT1

OC

GND

+5V_USBPO1

C294

220uF/6.3V_6X4.5

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OUT2

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VIN2

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OC

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C294

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5VSS

SUSON

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EN

OUT3

OUT2

OUT1

OC

GND

+5V_USBPO1

C294

220uF/6.3V_6X4.5

5VSS

SUSON

VIN1

VIN2

EN

OUT3

OUT2

OUT1

OC

GND

+5V_USBPO1

C294

220uF/6.3V_6X4.5

5VSS

SUSON

VIN1

VIN2

EN

OUT3

OUT2

OUT1

OC

GND

+5V_USBPO1

C294

220uF/6.3V_6X4.5

5VSS

SUSON

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VIN1

VIN2

EN

OUT3

OUT2

OUT1

OC

GND

+5V_USBPO1

C294

220uF/6.3V_6X4.5

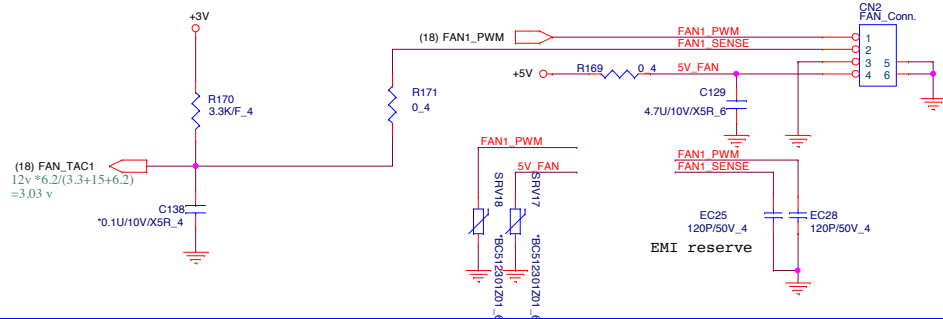
5VSS

SUSON

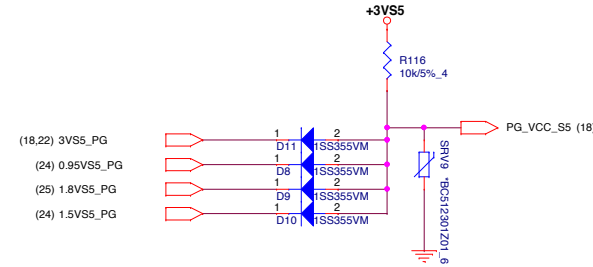
VIN1



SYSTEM FAN



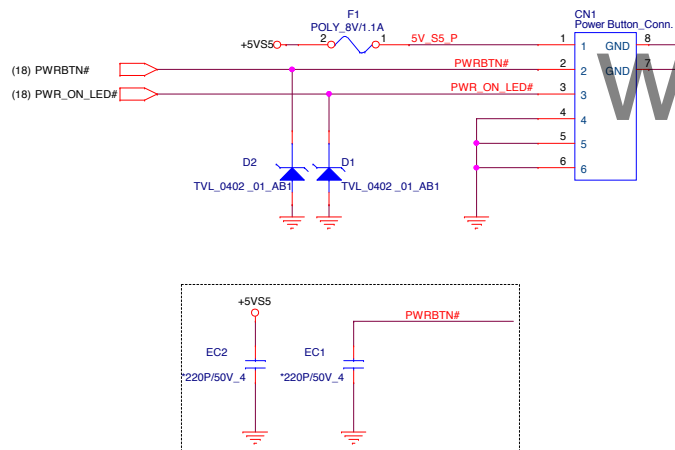
S5 POWER GOOD



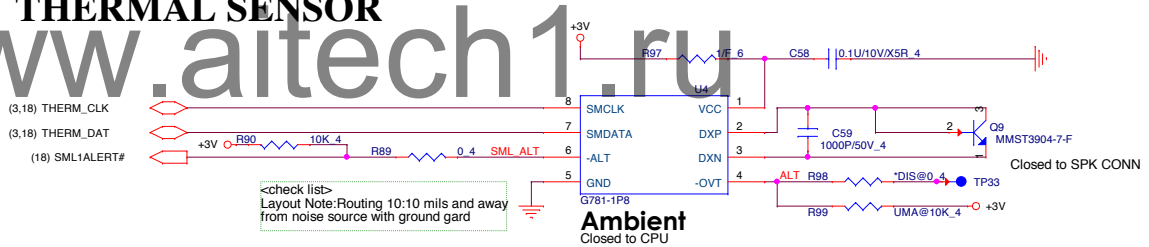
19

Power Button CONN

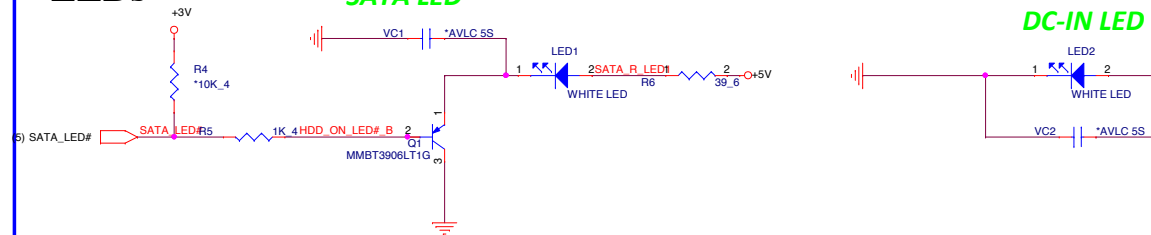
SW1 For Debug.MP will remove it.

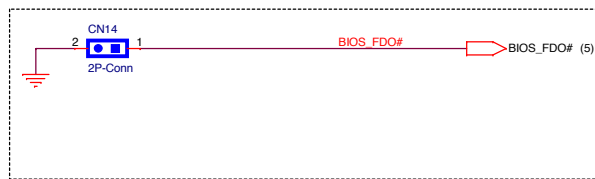


THERMAL SENSOR

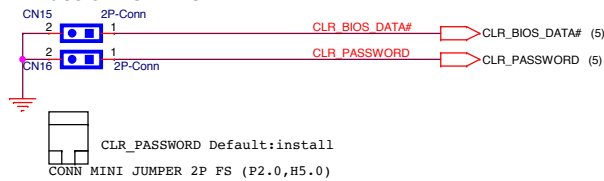


LEDs

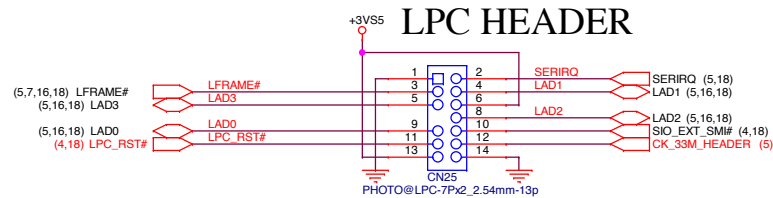




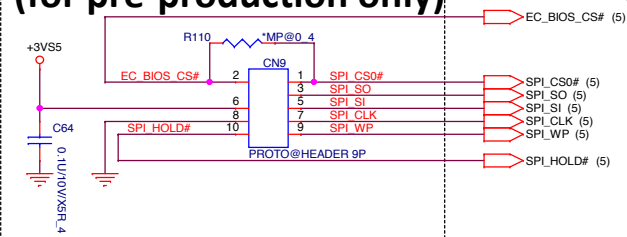
***Place on PCBA BOT**



(4,5,6,7,10,13,16,18,19,21,22,24,25,28) +3VS5



ROM recovery (for pre-production only)

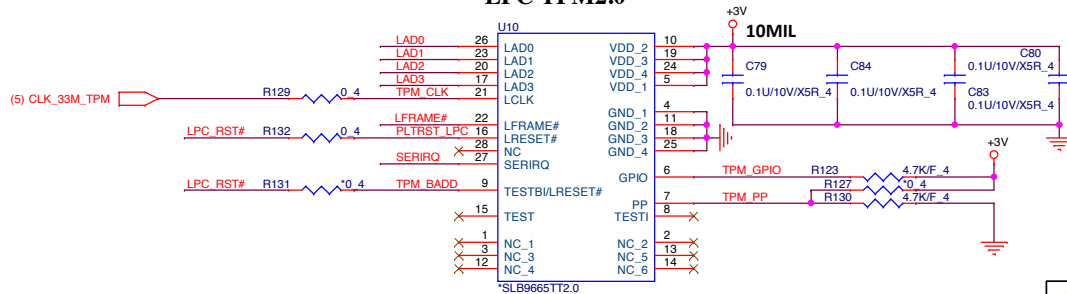


```

ON Chip select:Default:iinsatall (PROTO only)
CONN MINI JUMPER 2P FS (P2.0,H5.0)

```

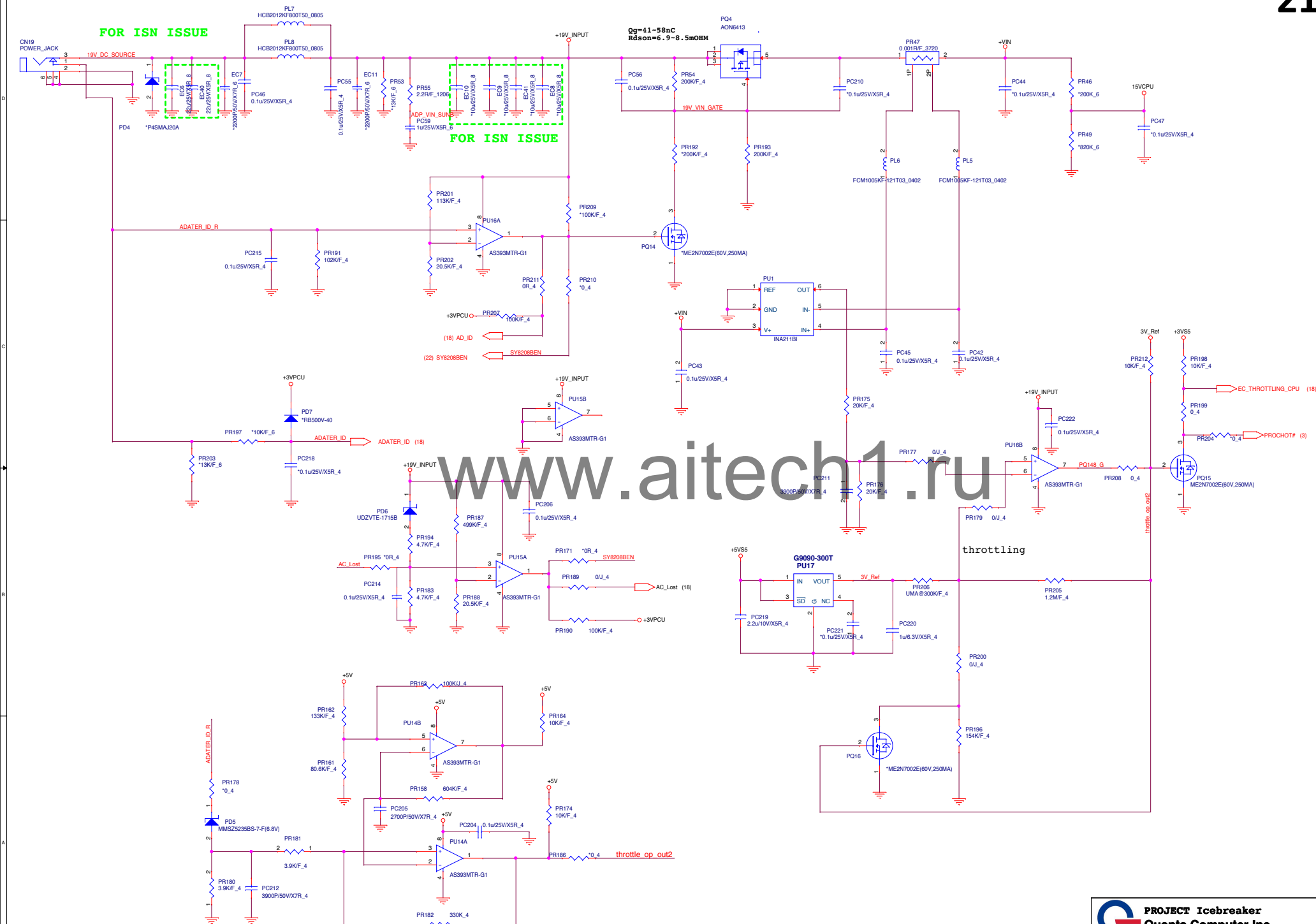
LPC TPM2.0

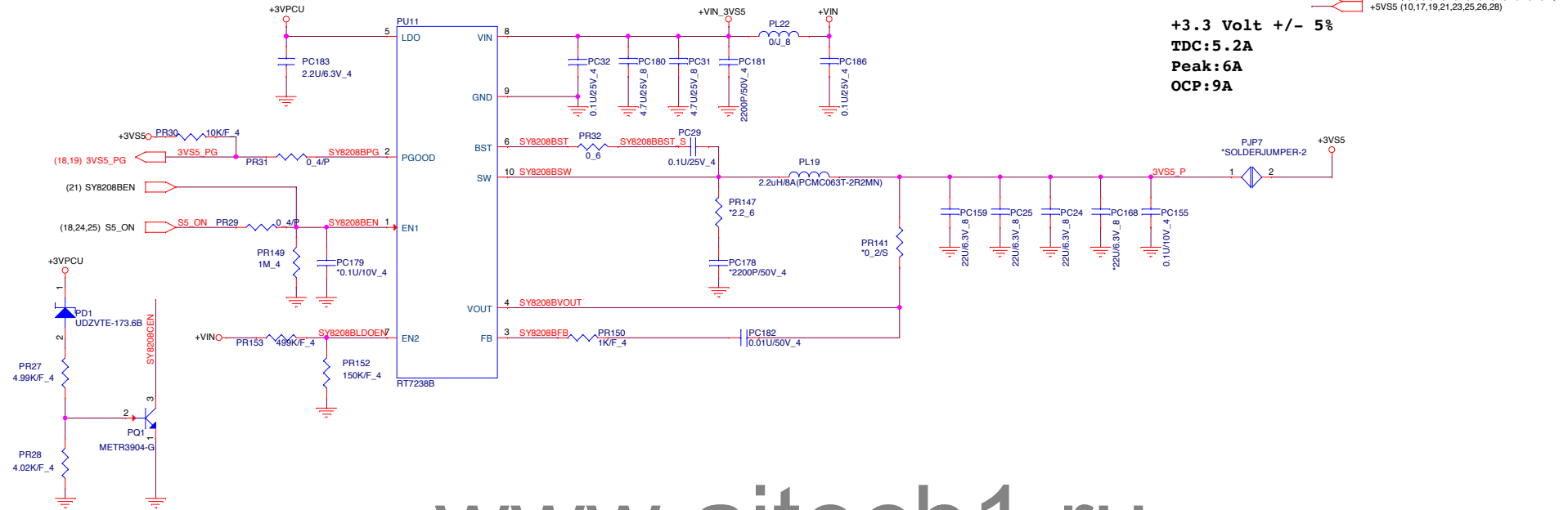


CLR_CMOS

Jumper	Pre-production	Production
BOOT_BLK_Recovery	X	X
BOOT_BLK_Enable	0	X

Jumper	Type
Pop	CLR BIOS DAT
Pop	CLR PASSWD
Pop	BOOT_BLK Recovery
Pop	BOOT_BLK Enable





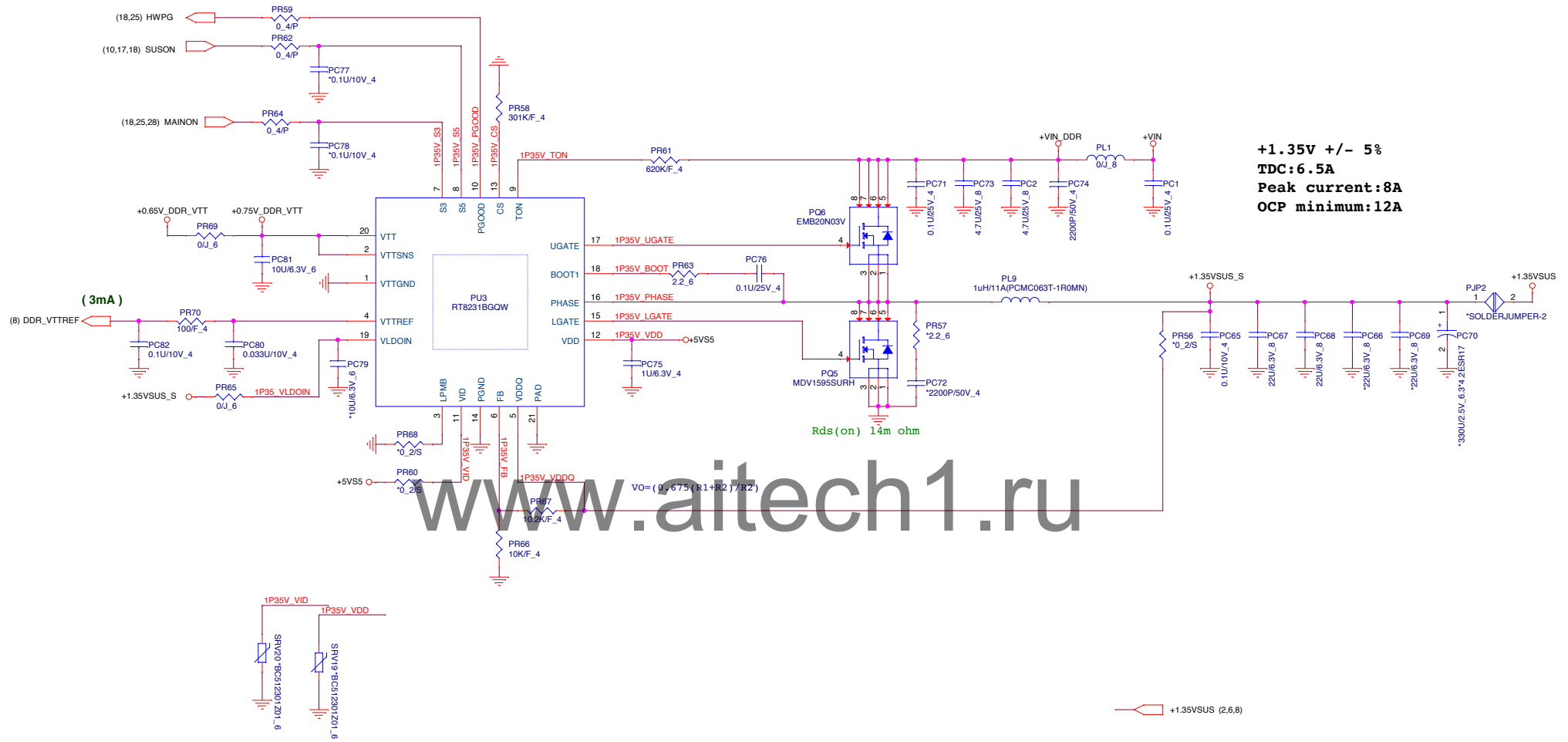
www.aitech1.ru

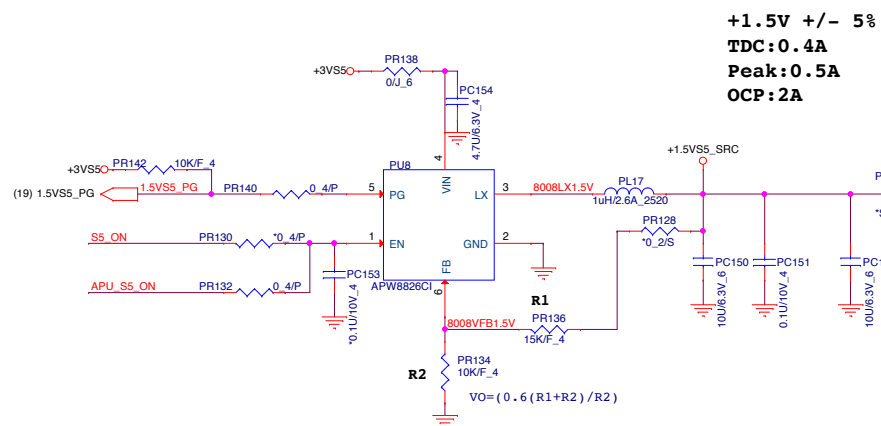
Reserve for USB Charge

USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

Do Not add test pad on VCC & LDO pin

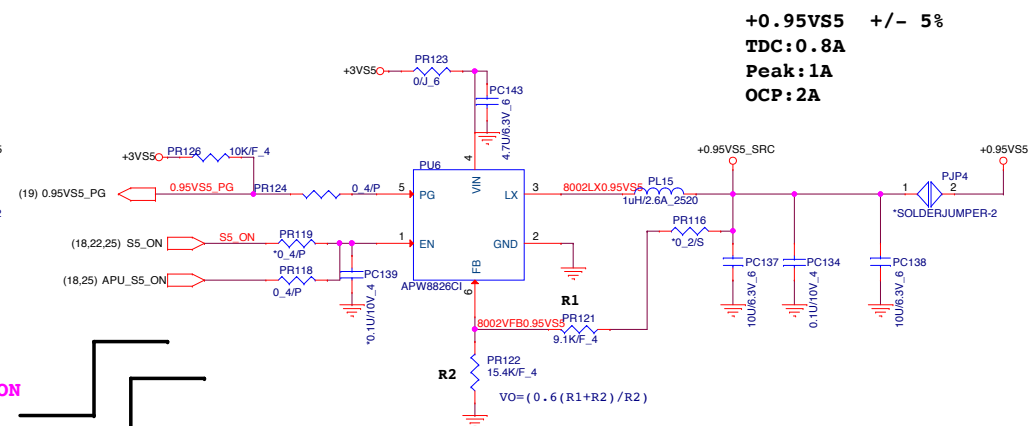
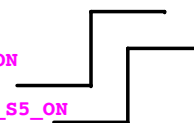
+5 Volt +/- 5%
TDC: 6.1A
Peak: 7.6A
OCP: 9A



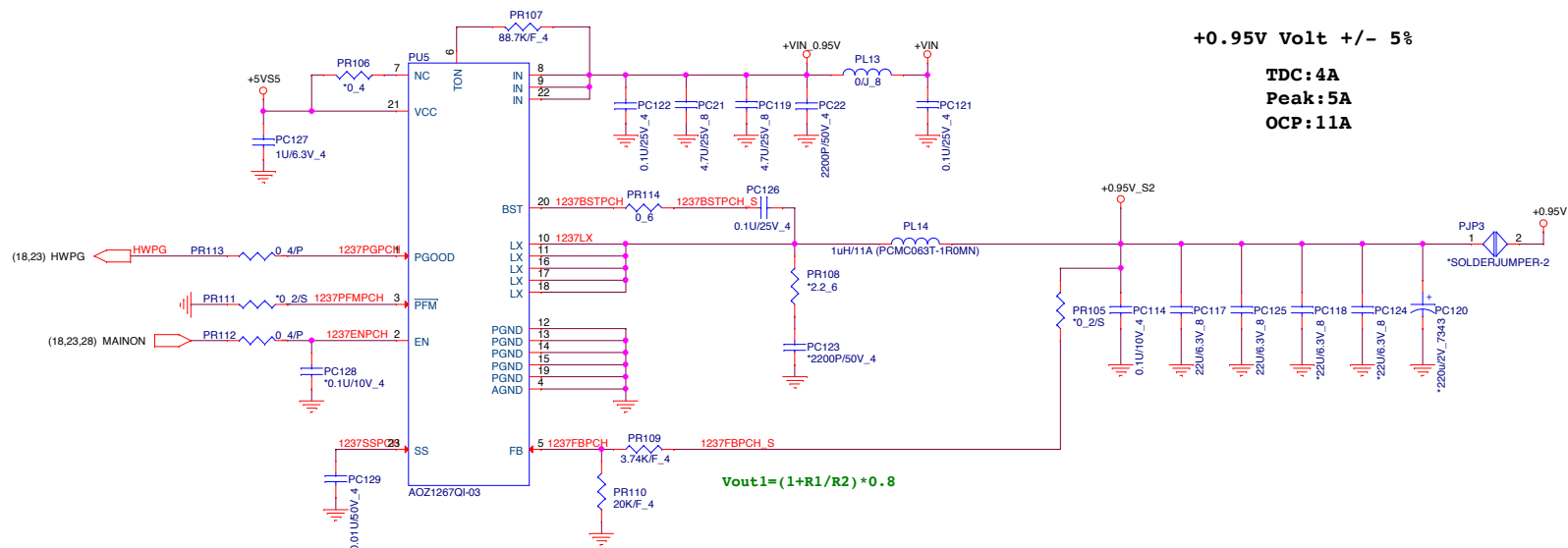


S5_ON

APU_S5_ON



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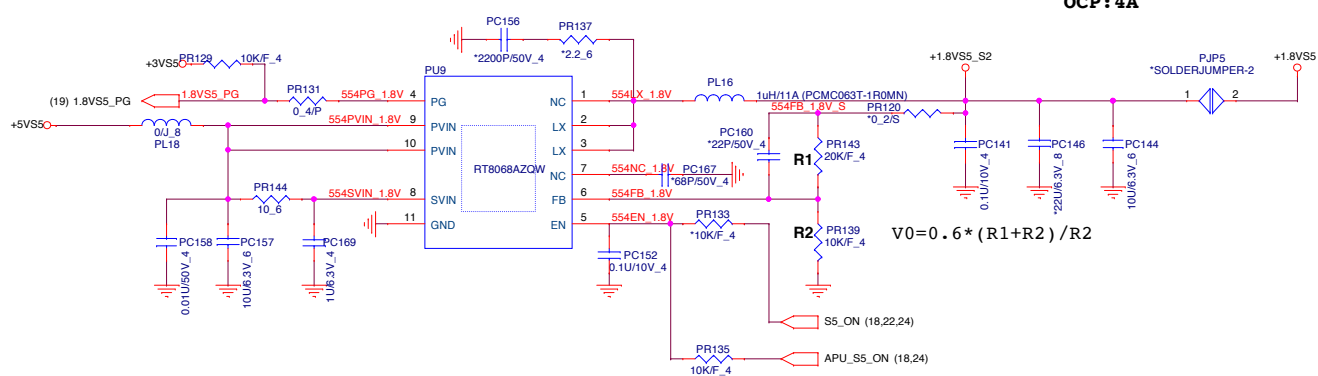
www.aitech1.ru

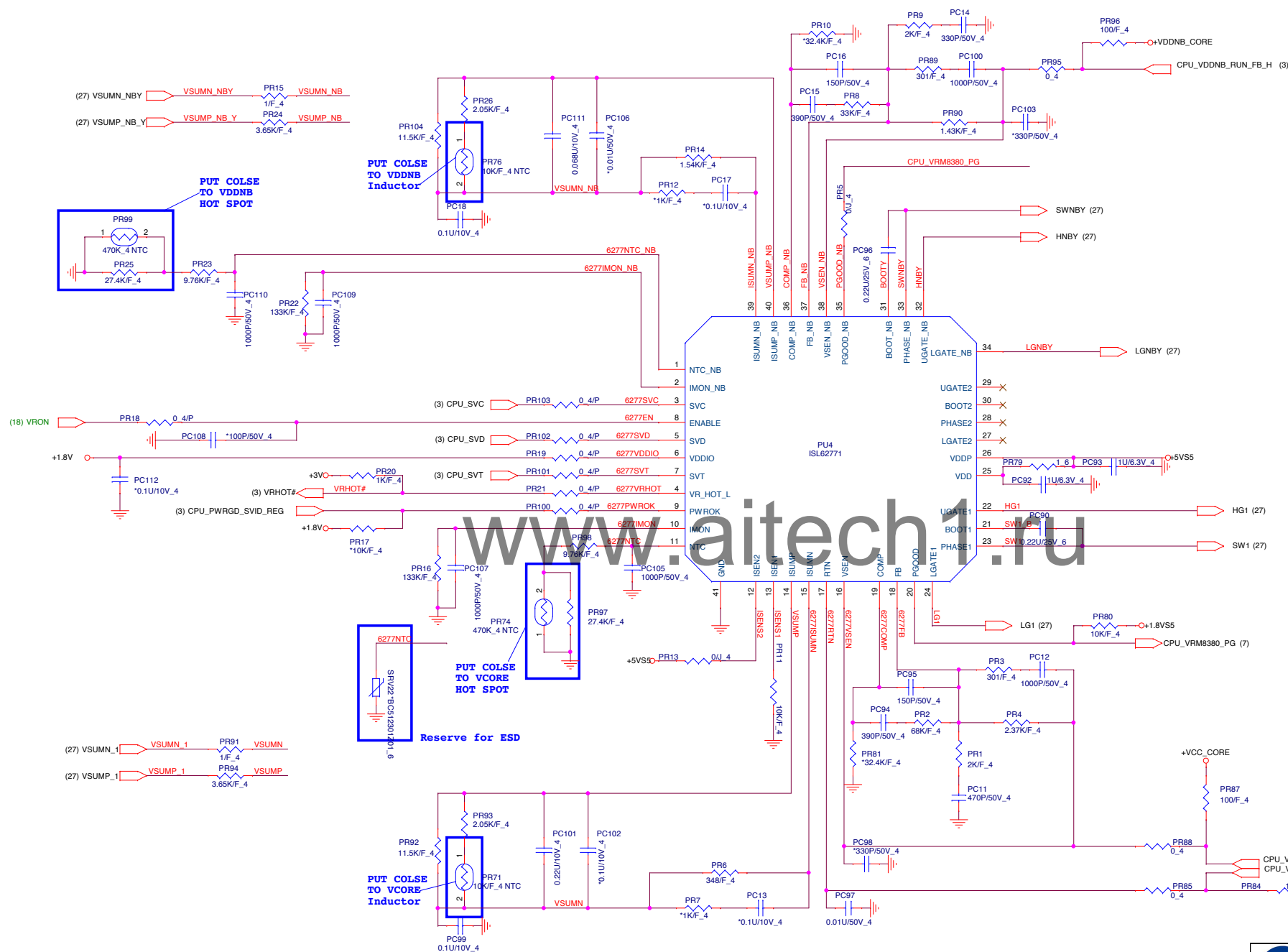
1.8VVS5 +/- 3%

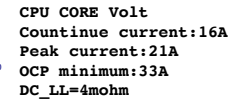
TDC: 1.6A

Peak: 2A

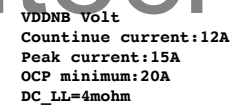
OCP: 4A

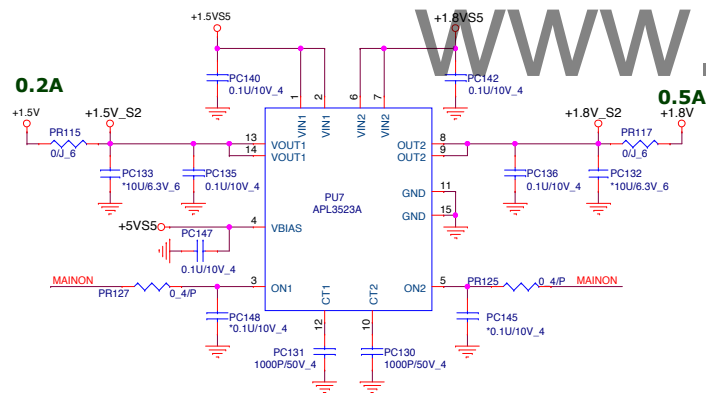
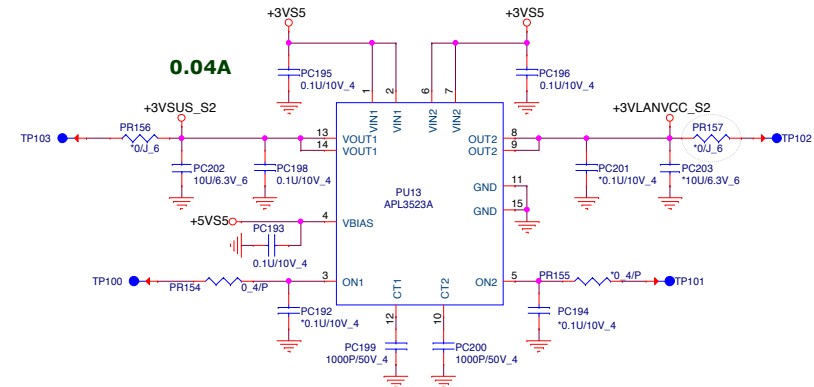
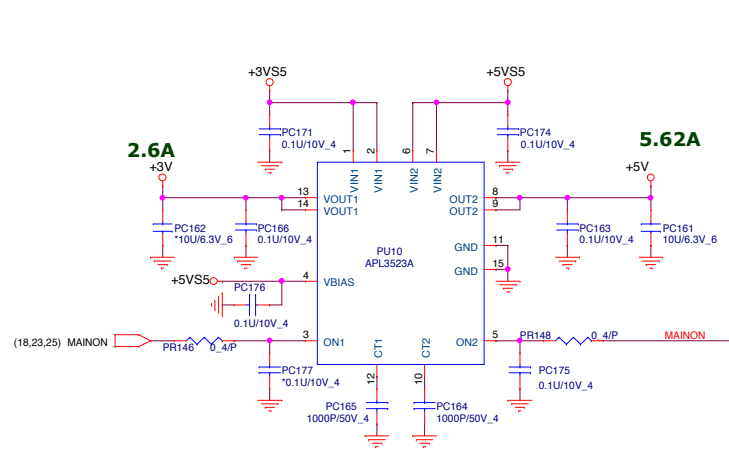


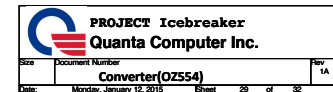




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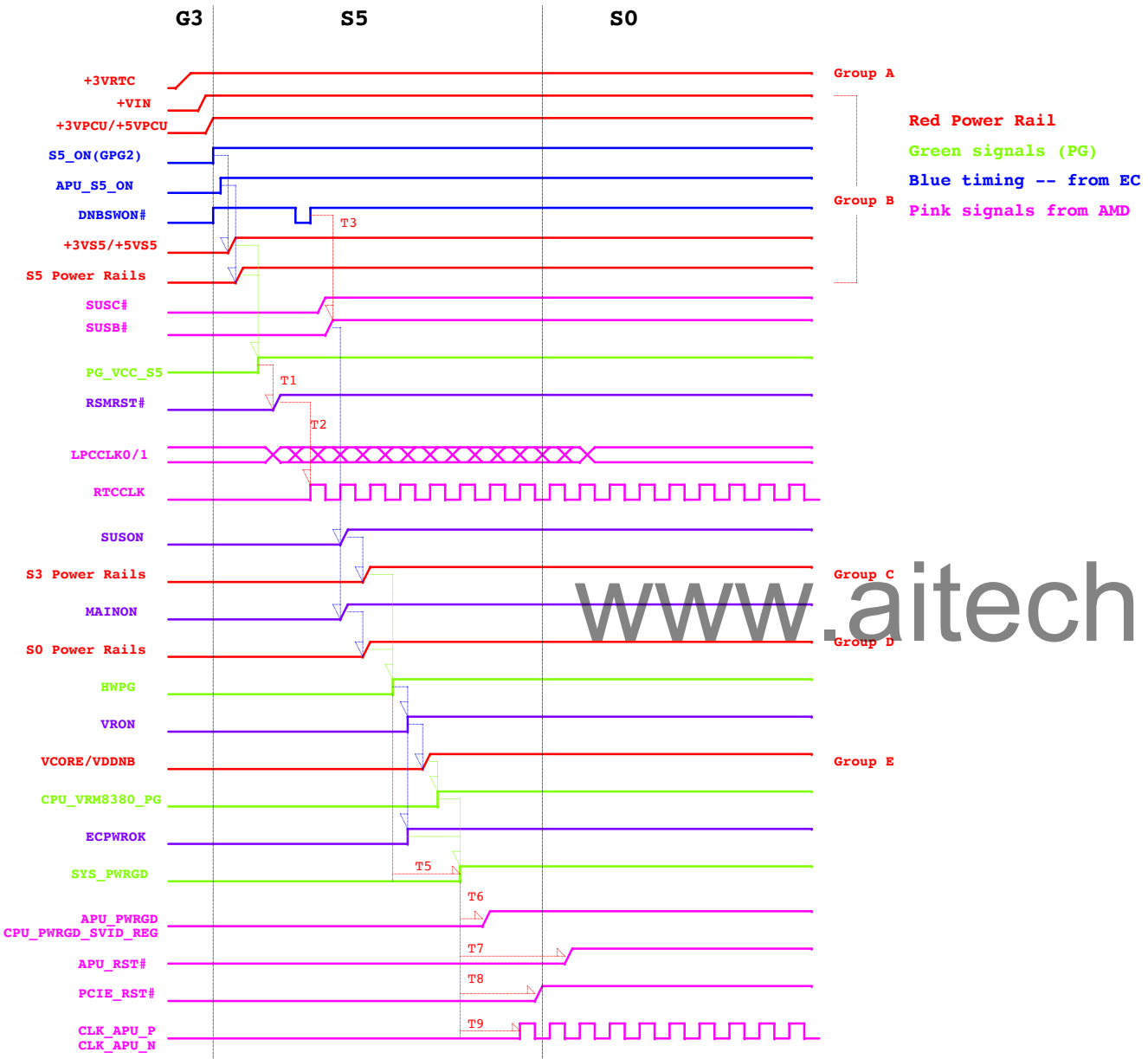




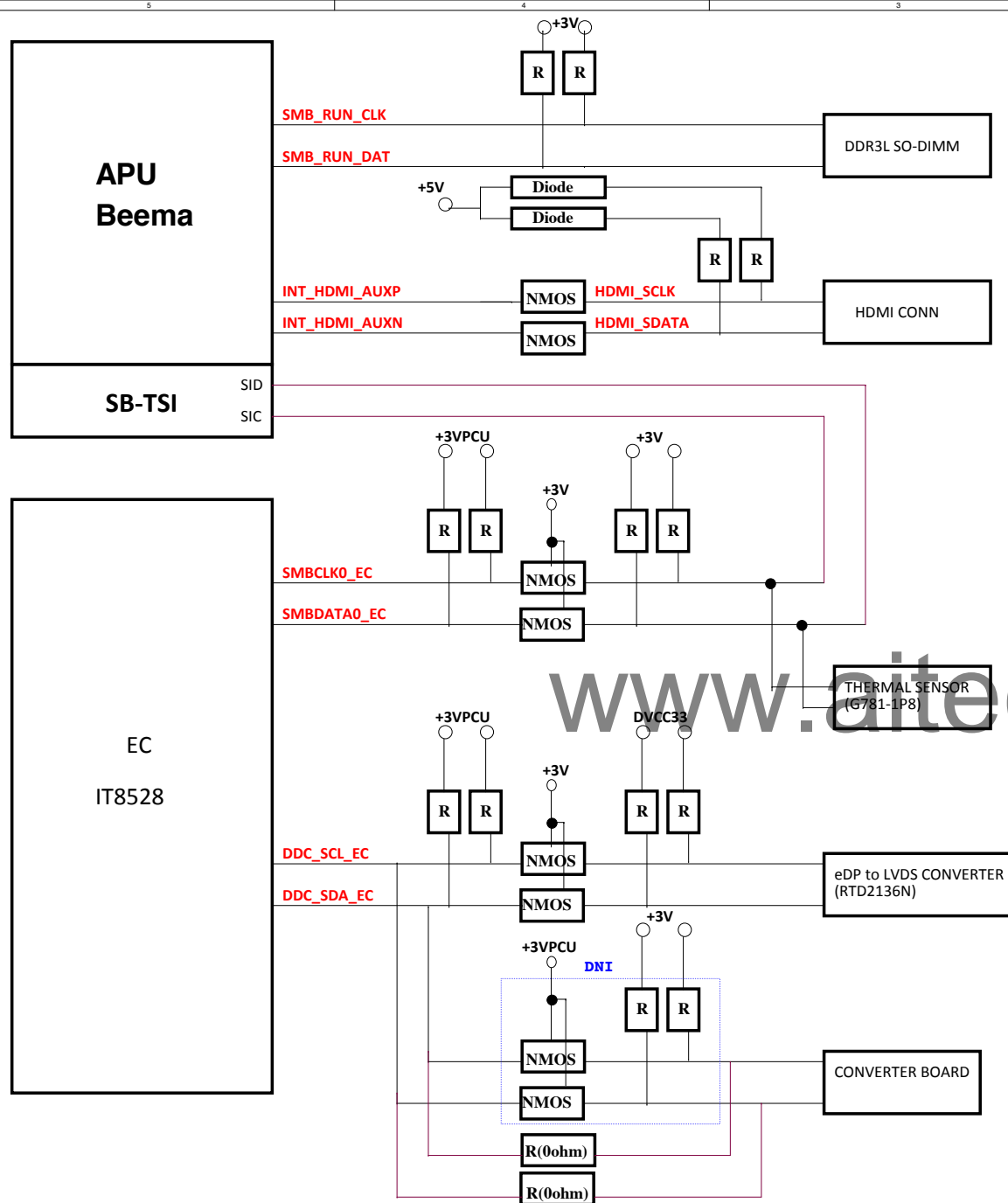


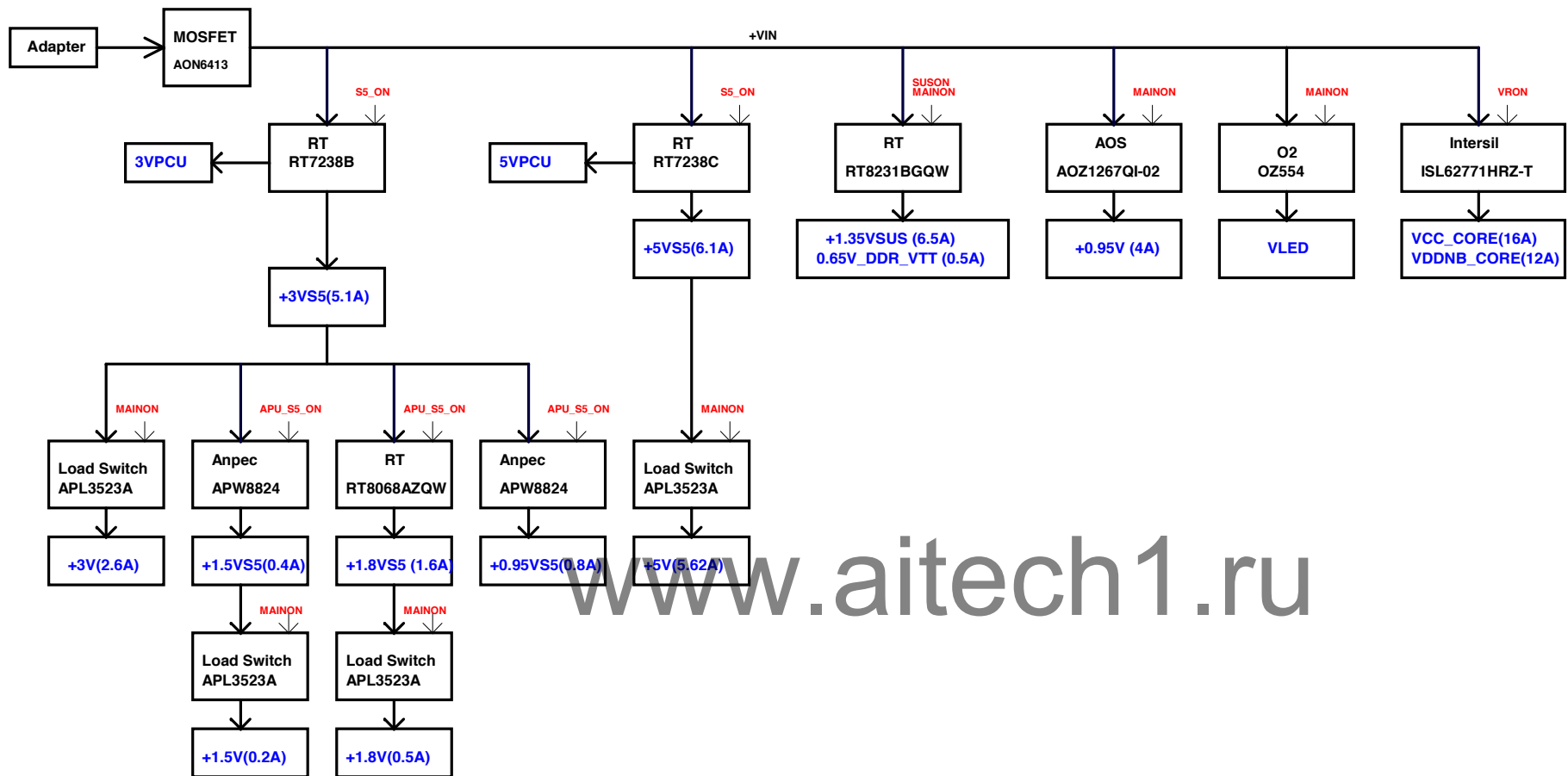
Beema Power on sequence

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